SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2015-173747; filed on September 03, 2015; the entire contents of which are incorporated herein by reference.

FIELD

Embodiments described herein relate generally to a semiconductor device including semiconductor chips which are stacked.

BACKGROUND

A semiconductor device is known in which multiple semiconductor chips (or semiconductor elements) are stacked in multiple stages.

An example of related art includes JP-A-2-273930.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagram illustrating a circuit configuration of a semiconductor device according to a first embodiment.

FIG. 2 is a diagram illustrating a structure of a semiconductor chip in the semiconductor device according to the first embodiment.

FIG. 3 is a diagram illustrating another structure of the semiconductor chip in the semiconductor device according to the first embodiment.

FIG. 4 is an enlarged diagram of a terminal section of the semiconductor chip according to the first embodiment.

FIG. 5 is a diagram illustrating a fabrication process of the semiconductor chip according to the first embodiment.

FIG. 6 is an enlarged diagram of the semiconductor chip illustrated in FIG. 5.

FIG. 7 is a diagram illustrating a scribe position of the semiconductor chip illustrated in FIG. 6.

FIG. 8 is an enlarged diagram of a terminal section of a semiconductor chip according to a second embodiment.

DETAILED DESCRIPTION

[0004]Embodiments are to provide a semiconductor device which can reduce abnormality of a connection made by a bonding wire between a lead terminal and a pad of a semiconductor chip stacked thereon.

[0005]In general, according to one embodiment, a semiconductor device includes a first terminal; a first semiconductor chip; a second semiconductor chip which is disposed on the first semiconductor chip; a first pad which is provided on the first semiconductor chip and is in a state of an electrical disconnection; a second pad which is provided on the second semiconductor chip and is in a state of an electrical connection; a first wire which connects the first terminal to the first pad; and a second wire which connects the first pad to the second pad.

[0007]Hereinafter, embodiments will be described with reference to the drawings. In the following description, the same reference numerals or symbols will be attached to configuration elements having the same function and configuration.

1. First Embodiment

1.1 Circuit Configuration of Semiconductor Device

[0008]A circuit configuration of a semiconductor device according to a first embodiment will be described with reference to FIG. 1.

As illustrated in FIG. 1, a semiconductor device 10 includes, for example, multiple semiconductor chips (or semiconductor elements) 11\_1, 11\_2, 11\_3, and 11\_4. Each of the semiconductor chips 11\_1 to 11\_4 includes a semiconductor substrate in which a semiconductor circuit, for example, a memory circuit, various drivers, an input and output circuit, and the like are formed. Here, a case in which the semiconductor device 10 includes four semiconductor chips is illustrated, but the semiconductor device 10 may also include five or more semiconductor chips. A semiconductor chip 11 indicates each of the four semiconductor chips 11\_1 to 11\_4.

[0009]A controller 12 is connected to each of the semiconductor chips 11\_1 to 11\_4. The controller 12 controls each of the semiconductor chips 11\_1 to 11\_4. The controller 12 outputs a chip enable signal CE1 to the semiconductor chip 11\_1. Furthermore, the controller 12 respectively outputs the chip enable signal CE2 to the semiconductor chip 11\_2, the chip enable signal CE3 to the semiconductor chip 11\_3, and the chip enable signal CE4 to the semiconductor chip 11\_4.

[0010]The chip enable signal CE1 makes the semiconductor chip 11\_1 to an operable state, or to an inoperable state. The chip enable signal CE2 makes the semiconductor chip 11\_2 to an operable state, or to an inoperable state. The chip enable signal CE3 makes the semiconductor chip 11\_3 to an operable state, or to an inoperable state. The chip enable signal CE4 makes the semiconductor chip 11\_4 to an operable state, or to an inoperable state.

[0011]In addition, the controller 12 outputs input and output signals IO0, IO1, IO2, IO3, IO4, IO5, IO6, and IO7 to each of the semiconductor chips 11\_1 to 11\_4. In addition, the controller 12 outputs other signals including a write enable signal WE and a read enable signal RE to each of the semiconductor chips 11\_1 to 11\_4.

1.2 Structure of Semiconductor Device

[0012]A structure of the semiconductor device according to the first embodiment will be described.

1.2.1 Stacking Structure of Semiconductor Chips

[0013]A stacking structure of semiconductor chips in the semiconductor device 10 will be described with reference to FIG. 2.

Each of the semiconductor chips 11\_1 to 11\_4 has a rectangular shape. A pad area 1A in which pads are disposed is disposed on a long side of the rectangular shape of the semiconductor chip 11\_1. In the same time, a pad area 2A in which pads are disposed is disposed on a long side of the rectangular shape of the semiconductor chip 11\_2. A pad area 3A in which pads are disposed is disposed on a long side of the rectangular shape of the semiconductor chip 11\_3, and a pad area 4A in which pads are disposed is disposed on a long side of the rectangular shape of the semiconductor chip 11\_4.

[0014]Semiconductor chips 11\_2, 11\_3, and 11\_4 are sequentially stacked on the semiconductor chip 11\_1 from the semiconductor chip 11\_1. The semiconductor chip 11\_2 is disposed on the semiconductor chip 11\_1 so as to be shifted by the pad area 1A of the semiconductor chip 11\_1. The semiconductor chip 11\_3 is disposed on the semiconductor chip 11\_2 so as to be shifted by the pad area 2A of the semiconductor chip 11\_2. Furthermore, the semiconductor chip 11\_4 is disposed on the semiconductor chip 11\_3 so as to be shifted by the pad area 3A of the semiconductor chip 11\_3.

1.2.2 Another Stacking Structure of semiconductor Chips

[0015]Another stacking structure of semiconductor chips will be described with reference to FIG. 3.

The pad area 1A is disposed on a short side of the rectangular shape of the semiconductor chip 11\_1. The pad area 3A is disposed on a short side of the rectangular shape of the semiconductor chip 11\_3. In addition, the pad area 2A is disposed on a long side of the rectangular shape of the semiconductor chip 11\_2. The pad area 4A is disposed on a long side of the rectangular shape of the semiconductor chip 11\_4.

[0016]The semiconductor chip 11\_2 is disposed on the semiconductor chip 11\_1 so as to be shifted by the pad area 1A of the semiconductor chip 11\_1. The semiconductor chip 11\_3 is disposed on the semiconductor chip 11\_2 so as to be shifted by the pad area 2A of the semiconductor chip 11\_2. Furthermore, the semiconductor chip 11\_4 is disposed on the semiconductor chip 11\_3 so as to be shifted by the pad area 3A of the semiconductor chip 11\_3.

[0017]That is, as illustrated in FIG. 3, the pad area 2A on the long side of the semiconductor chip 11\_2 is disposed so as to correspond to the pad area 1A on the short side of the semiconductor chip 11\_1. Furthermore, the pad area 3A on the short side of the semiconductor chip 11\_3 is disposed so as to correspond to the pad area 2A of the semiconductor chip 11\_2, and the pad area 4A on the short side of the semiconductor chip 11\_4 is disposed so as to correspond to the pad area 3A of the semiconductor chip 11\_3.

1.2.3 Configuration of Pad of Semiconductor Chip

[0018]A configuration of pads of semiconductor chips illustrated in FIG. 2 and FIG. 3 will be described with reference to FIG. 4.

The pad area 1A of the semiconductor chip 11\_1 includes two columns in which pads are disposed. A signal pad 1S is disposed in a column (first column) on a center side of the semiconductor chip 11\_1. The signal pad 1S is a pad which a signal is input to and output from, is electrically connected to the semiconductor chip 11\_1, and is in a state of an electrical connection. For example, the chip enable signal CE1, the write enable signal WE, the read enable signal RE, or the input and output signals IO0 to IO7 are input to and output from to the signal pad 1S. In addition, a dummy pad 1D is disposed in a column (second column) on an end portion side of the semiconductor chip 11\_1. The dummy pad 1D is disposed in a scribe area which will be described below, is not electrically connected to a circuit of, for example, the semiconductor chip 11\_1, and is in a state of an electrical disconnection.

[0019]In the same manner, the pad area 2A of the semiconductor chip 11\_2 includes two columns in which pads are disposed. A signal pad 2S is disposed in a column on a center side of the semiconductor chip 11\_2. The signal pad 2S is a pad which a signal is input to and output from, is electrically connected to the semiconductor chip 11\_2, and is in a state of an electrical connection. For example, the chip enable signal CE2, the write enable signal WE, the read enable signal RE, or the input and output signals IO0 to IO7 are input to and output from to the signal pad 2S. A dummy pad 2D is disposed in a column on an end portion side of the semiconductor chip 11\_2. The dummy pad 2D is disposed in the scribe area, is not electrically connected to a circuit of, for example, the semiconductor chip 11\_2, and is in a state of an electrical disconnection.

[0020]The pad area 3A of the semiconductor chip 11\_3 includes two columns in which pads are disposed. A signal pad 3S is disposed in a column on a center side of the semiconductor chip 11\_3. The signal pad 3S is a pad which a signal is input to and output from, is electrically connected to the semiconductor chip 11\_3, and is in a state of an electrical connection. For example, the chip enable signal CE3, the write enable signal WE, the read enable signal RE, or the input and output signals IO0 to IO7 are input to and output from to the signal pad 3S. A dummy pad 3D is disposed in a column on an end portion side of the semiconductor chip 11\_3. The dummy pad 3D is disposed in a scribe area, is not electrically connected to a circuit of, for example, the semiconductor chip 11\_3, and is in a state of an electrical disconnection.

[0021]The pad area 4A of the semiconductor chip 11\_4 includes two columns in which pads are disposed. A signal pad 4S is disposed in a column on a center side of the semiconductor chip 11\_4. The signal pad 4S is a pad which a signal is input to and output from, is electrically connected to the semiconductor chip 11\_4, and is in a state of an electrical connection. For example, the chip enable signal CE4, the write enable signal WE, the read enable signal RE, or the input and output signals IO0 to IO7 are input to and output from to the signal pad 4S. A dummy pad 4D is disposed in a column on an end portion side of the semiconductor chip 11\_4. The dummy pad 4D is disposed in a scribe area, is not electrically connected to a circuit of, for example, the semiconductor chip 11\_4, and is in a state of an electrical disconnection.

[0022]In addition, as illustrated in FIG. 4, multiple lead terminals for an electrical connection to the outside are disposed on an outer side of the pad area 1A of the semiconductor chip 11\_1. Here, four lead terminals 21\_1, 21\_2, 21\_3, and 21\_4 are illustrated. Wires 22 to 29 are connected between the lead terminals and the pads, or pads. The connections made by the wires will be described below.

1.2.4 Connection between pad and lead terminal of Semiconductor Chip

[0023]Connections made by wires between pads of the semiconductor chip 11 and lead terminals will be described with reference to FIG. 4.

First, an example in which a connection between the lead terminal 21\_1 and the signal pad 4S is made by a wire will be described. For example, the chip enable signal CE4 is transferred from the lead terminal 21\_1 to the signal pad 4S.

[0024]A wire 22 is bonded between the lead terminal 21\_1 and the dummy pad 1D. As a result, the lead terminal 21\_1 is electrically connected to the dummy pad 1D. Furthermore, a wire 23 is bonded between the dummy pad 1D and the dummy pad 2D, and the dummy pad 1D is electrically connected to the dummy pad 2D. A wire 24 is bonded between the dummy pad 2D and the dummy pad 3D, and the dummy pad 2D is electrically connected to the dummy pad 3D. Furthermore, a wire 25 is bonded between the dummy pad 3D and the signal pad 4S, and the dummy pad 3D is electrically connected to the signal pad 4S.

[0025]For example, the chip enable signal CE4 is supplied to the lead terminal 21\_1 from the controller 12. The chip enable signal CE4 is transferred to the signal pad 4S from the lead terminal 21\_1 through the wire 22, the dummy pad 1D, the wire 23, the dummy pad 2D, the wire 24, the dummy pad 3D, and the wire 25.

[0026]Here, the wires are connected to the signal pad 4S from the lead terminal 21\_1 through the dummy pads 1D, 2D, and 3D. That is, in order to connect a wire between the lead terminal 21\_1 and the signal pad 4S, the dummy pads 1D, 2D, and 3D are used as relay pads of connections made by wires. As a result, it is possible to reduce a length of each of the wires 22 to 25, compared to a case in which the lead terminal 21\_1 is directly connected to the signal pad 4S by a wire. As a result, it is possible to reduce abnormality in which a wire is deformed due to moving the left and right, or a wire is disconnected from a lead terminal or a pad.

[0027]Next, an example in which a wire is connected between the lead terminal 21\_3 and signal pads 1S to 4S will be described. In this example, for example, the input signal IO0 is transferred to each of the signal pads 1S to 4S from the lead terminal 21\_3.

[0028]A wire 26 is bonded between the lead terminal 21\_3 and the signal pad 1S. As a result, the lead terminal 21\_3 is electrically connected to the signal pad 1S. Furthermore, a wire 27 is bonded between the signal pad 1S and the signal pad 2S, and the signal pad 1S is electrically connected to the signal pad 2S. A wire 28 is bonded between the signal pad 2S and the signal pad 3S, and the signal pad 2S is electrically connected to the signal pad 3S. Furthermore, a wire 29 is bonded between the signal pad 3S and the signal pad 4S, and the signal pad 3S is electrically connected to the signal pad 4S.

[0029]For example, the input and output signal IO0 is supplied to the lead terminal 21\_3 from the controller 12. The input and output signal IO0 is transferred to the signal pad 1S from the lead terminal 21\_3 through the wire 26. Furthermore, the input and output signal IO0 is transferred to the signal pad 2S through the wire 27. Furthermore, the input and output signal IO0 is transferred to the signal pad 3S through the wire 28 and is transferred to the signal pad 4S through the wire 29.

[0030]Here, in order to connect between the lead terminal 21\_3 and each of the signal pads 1S to 4S using wires, wires are sequentially connected between the lead terminal 21\_3 and the signal pad 1S, between the signal pad 1S and the signal pad 2S, between the signal pad 2S and the signal pad 3S, and the signal pad 3S and the signal pad 4S. For this reason, wires which are connected between the lead terminal 21\_3 and a signal pad, and between signal pads are not lengthened, and abnormality of connections made by wires hardly occurs.

1.3 Manufacturing Method of Semiconductor Device

[0031]A fabrication method of the semiconductor chip 11 in the semiconductor device 10 will be described with reference to FIGS. 5, 6, and 7.

[0032]FIG. 5 illustrates an enlarged diagram of a part of the semiconductor chips 11 whose layout is made on a wafer. Layout of the semiconductor chips 11 is made on a wafer. Scribe areas (Kerf area) 31 are provided between semiconductor chips 11 so as to separate the semiconductor chips.

[0033]FIG. 6 illustrates an enlarged diagram of the semiconductor chip 11. A memory circuit, various drivers, an input and output circuit, and the like are formed in a central area of the semiconductor chip 11. Positioning marks 32 for photolithography, pads 1T (or 2T, 3T, or 4T) of a test element group (TEG) element, and dummy pads 1D (or 2D, 3D, or 4D) are disposed in the scribe areas 31. The TEG element indicates a test element for assessing elements formed on the semiconductor chip. The dummy pad 1D within a dashed line A is disposed on an end portion side rather than a pad of the TEG element. The dummy pad 1D in a dashed line B is disposed on a central area side rather than the pad of the TEG element.

[0034]In a scribe process, the semiconductor chips 11 are separated by shifting a scribe area 31A such that the dummy pad 1D provided in the scribe areas 31 remains on the semiconductor chip 11, as illustrated in FIG. 7. As a result, the scribe areas 31 on which the dummy pads 1D are disposed can remain on the semiconductor chip 11.

[0035]Thereafter, the semiconductor chips 11 are stacked, and thus the semiconductor chips which are stacked in multiple stages are formed. Furthermore, wire bonding is performed between lead terminals and pads of the semiconductor chip, and the semiconductor chips are sealed with a resin, and thus the semiconductor device (package) 10 is formed.

1.4 Effects of First Embodiment

[0036]According to the first embodiment, it is possible to provide a semiconductor device which can reduce abnormality of connections made by wire bonding between pads of stacked semiconductor chips and lead terminals. Furthermore, relay pads for connecting bonding wires are disposed in scribe areas, and thus it is possible to prevent an area of a semiconductor chip from increasing.

[0037]Hereinafter, the effects of the first embodiment will be described in detail using a comparison example.

[0038]For example, in a semiconductor device in which semiconductor chips are stacked in multiple stages, wires are required to be connected across pads provided in each semiconductor chip, if wires are connected to the second or the next semiconductor chips from lead terminals. In this case, bonding wires are lengthened, and flow or disconnection of the wires easily occur at the time of sealing with resin. Furthermore, if large scaling or large capacity of circuits is required, the number of stages of semiconductor chips which are stacked is increased, and thus a length of the wire is further lengthened, and there is a high possibility that flow or disconnection of the wire occurs.

[0039]For this reason, for example, dummy pads are disposed in an area in which signal pads of a semiconductor chip are disposed, the dummy pads are used as relay pads for connecting bonding wires, and thus it is possible to prevent the bonding wires from being lengthened. However, if the semiconductor chip is miniaturized and an area of the semiconductor chip is reduced, surplus pads are hardly disposed in the semiconductor chip. That is, if the semiconductor chip is miniaturized, dummy pads are hardly disposed in the area in which the signal pads are disposed due to limitation of a chip size.

[0040]Hence, in the first embodiment, dummy pads are formed in a scribe area in the outside of an area in which signal pads of a semiconductor chip are disposed. Thus, the dummy pads formed in the scribe area are used as relay pads for connecting the bonding wires. That is, when a wire is connected to a pad of a connection target, the wire is not directly connected to the pad of the connection target from a lead terminal of a package substrate, the wire is first connected to the dummy pad of the scribe area from the lead terminal, and next, the wire is connected to the pad of the connection target from the dummy pad. A connection between the lead terminal and the pad of the connection target may be made through multiple dummy pads. As a result, it is possible to prevent the bonding wire from being lengthened, and to reduce abnormality in which a wire is deformed due to moving to the left and right when sealing with a resin, or a wire is disconnected from a lead terminal or a pad.

[0041]Furthermore, it is possible to prevent a size of an area in which signal pads are disposed from increasing, by forming the dummy pads in the scribe area in the outside of an area in which the signal pads are disposed. As a result, it is possible to prevent a size of a semiconductor chip and a semiconductor device from increasing.

2. Second Embodiment

[0042]In a second embodiment, pads of a TEG element provided in a scribe area are used as relay pads for connecting bonding wires. In the second embodiment, points different from those in the first embodiment will be described.

2.1 Configuration of Semiconductor Chip

[0043]A configuration of pads of a semiconductor chip will be described with reference to FIG. 8. FIG. 4 illustrates a pad area of the semiconductor chips 11\_1 to 11\_4 and a part of lead terminals.

[0044]Pads (hereinafter, TEG pads) 1T of a TEG element are disposed in a column on an end portion side of the semiconductor chip 11\_1. The TEG pads 1T are disposed in a scribe area 31, and are electrically connected to the TEG element.

[0045]In the same manner, TEG pads 2T are disposed in a column on an end portion side of the semiconductor chip 11\_2. The TEG pads 2T are disposed in a scribe area 31, and are electrically connected to the TEG element.

[0046]TEG pads 3T are disposed in a column on an end portion side of the semiconductor chip 11\_3. The TEG pads 3T are disposed in a scribe area 31, and are electrically connected to the TEG element.

[0047]TEG pads 4T are disposed in a column on an end portion side of the semiconductor chip 11\_4. The TEG pads 4T are disposed in a scribe area 31, and are electrically connected to the TEG element.

2.2 Connection between Pads of Semiconductor Chip and Lead Terminal

[0048]Connections made by wires between pads of the semiconductor chip 11 and lead terminals will be described with reference to FIG. 8.

An example in which a wire is connected between a lead terminal 21\_1 and a signal pad 4S will be described. A wire 41 is bonded between the lead terminal 21\_1 and the TEG pad 1T, and the lead terminal 21\_1 is electrically connected to the TEG pad 1T. Furthermore, a wire 42 is bonded between the TEG pad 1T and a TEG pad 2T, and the TEG pad 1T is electrically connected to the TEG pad 2T. A wire 43 is bonded between the TEG pad 2T and a TEG pad 3T, and the TEG pad 2T is electrically connected to the TEG pad 3T. Furthermore, a wire 44 is bonded between the TEG pad 3T and the signal pad 4S, and the TEG pad 3T is electrically connected to the signal pad 4S.

[0049]For example, the chip enable signal CE4 which is output from the controller 12 is supplied to the lead terminal 21\_1. The chip enable signal CE4 is transferred to the signal pad 4S from the lead terminal 21\_1 through the wire 41, the TEG pad 1T, the wire 42, the TEG pad 2T, the wire 43, the TEG pad 3T, and the wire 44.

[0050]Here, the wires are connected to the signal pad 4S from the lead terminal 21\_1 through the TEG pads 1T, 2T, and 3T. That is, in order to connect a wire between the lead terminal 21\_1 and the signal pad 4S, the TEG pads 1T, 2T, and 3T are used as relay pads of connections made by wires. As a result, it is possible to reduce a length of each of the wires 41 to 44, compared to a case in which the lead terminal 21\_1 is directly connected to the signal pad 4S by a wire. As a result, it is possible to reduce abnormality in which a wire is deformed due to moving the left and right, or a wire is disconnected from a lead terminal or a pad.

2.3 Effects of Second Embodiment

[0051]According to the second embodiment, it is possible to use pads of a TEG element which are disposed in a scribe area of a semiconductor chip as relay pads for connecting bonding wires. In this case, it is possible to reduce a size of the scribe area and to ensure relay pads, even if dummy pads are hardly disposed in the scribe area.

[0052]Specifically, when a wire is connected to a pad of a connection target, the wire is not directly connected to the pad of the connection target from a lead terminal of a package substrate, the wire is first connected to the TEG pad from the lead terminal, and next, the wire is connected to the pad of the connection target from the TEG pad. A connection between the lead terminal and the pad of the connection target may be made through multiple TEG pads. As a result, it is possible to prevent the bonding wire from being lengthened, and to reduce abnormality in which a wire is deformed due to moving to the left and right when sealing with a resin, or a wire is disconnected from a lead terminal or a pad.

[0053]Furthermore, it is possible to prevent a size of an area in which signal pads are disposed from increasing, by using the TEG pads disposed in the scribe area as relay pads. As a result, it is possible to prevent a size of a semiconductor chip and a semiconductor device from increasing.

Modification Example or the Like

[0054]The first and second embodiments can be applied to, for example, various semiconductor devices which transmit signals from a controller to multiple semiconductor chips, regardless of a non-volatile memory (for example, NAND flash memory), a volatile memory, a system LSI, or the like.

[0055]While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first terminal;

a first semiconductor chip;

a second semiconductor chip which is disposed on the first semiconductor chip;

a first pad which is provided on the first semiconductor chip and is in a state of an electrical disconnection;

a second pad which is provided on the second semiconductor chip and is in a state of an electrical connection;

a first wire which connects the first terminal to the first pad; and

a second wire which connects the first pad to the second pad.

2. A semiconductor device comprising:

a first terminal;

a first semiconductor chip;

a second semiconductor chip which is disposed on the first semiconductor chip;

a first pad which is provided on the first semiconductor chip and is electrically connected to a test element;

a second pad which is provided on the second semiconductor chip and is in a state of an electrical connection;

a first wire which connects the first terminal to the first pad; and

a second wire which connects the first pad to the second pad.

3. The device according to Claim 1 or 2, wherein the first pad is disposed in a scribe area of the first semiconductor chip.

4. The device according to any one of Claims 1 to 3, further comprising:

a third pad which is provided on the first semiconductor chip and is in a state of an electrical connection,

wherein the first pad is disposed between the first terminal and the third pad.

5. The device according to any one of Claims 1 to 4, wherein the first pad is disposed between the first terminal and the second pad.

6. The device according to any one of Claims 1 to 5, wherein a signal which is transferred from the first terminal to the second pad includes a chip enable signal.

ABSTRACT

According to an embodiment, a semiconductor device includes a terminal, semiconductor chips which are stacked, and wires. Dummy pads and signal pads are disposed in the semiconductor chips. The wires connect the terminal to the pads. The wire connect the pads to each other.

Drawings

FIG. 1

12: CONTROLLER

11\_1 TO 11\_4: SEMICONDUCTOR CHIP

FIG. 5

11: SEMICONDUCTOR CHIP

FIG. 6

11: SEMICONDUCTOR CHIP

FIG. 7

11: SEMICONDUCTOR CHIP